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Walter L. Lindsay, Jr.	2812	
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	Examiner Walter L. Lindsay, Jr. Pars on the cover she t with to (OR REMAINS) CLOSED in this or other appropriate communication is subject and MPEP 1308. Raminer. Inder 35 U.S.C. § 119(a)-(d) or (for the been received. Inder abeen received in Application Note the application. Inder this communication to file a reference of this application. Inder the attached EXAMIT est be submitted. Inder the son's Patent Drawing Review (For the beader according to 37 CFR 1. Inder the beader according to 37 CFR 1. Index the beader according to 37 CFR 1.	Examiner Walter L. Lindsay, Jr. BAUKUS ET AL. Art Unit 2812 Bears on the cover she t with the correspondence address (OR REMAINS) CLOSED in this application. If not included or other appropriate communication will be mailed in due of IGHTS. This application is subject to withdrawal from issue 8 and MPEP 1308. Raminer. Inder 35 U.S.C. § 119(a)-(d) or (f). Be been received. Be been received in Application No. Cuments have been received in this national stage application of this communication to file a reply complying with the requirements of this application. But the stack of Examiner's AMENDMENT or NO es reason(s) why the oath or declaration is deficient. But the beader according to 37 CFR 1.121(d). But of BIOLOGICAL MATERIAL must be submitted. No FOR THE DEPOSIT OF BIOLOGICAL MATERIAL. Son's Patent Application (PTO-6. ☐ Interview Summary (PTO-413), Paper No./Mail Date

Application/Control Number: 10/619,981 Page 2

Art Unit: 2812

DETAILED ACTION

Allowable Subject Matter

1. Claims 5-8 and 13-14 are allowed.

2. The following is an examiner's statement of reasons for allowance: the prior art,

either singly or in combination fails to anticipate or render obvious, the limitations of:

... forming first and second buried silicon regions of a second conductivity type

within the silicon substrate of the first conductivity type;

depositing a first polycrystaliline silicon layer, said first polycrystalline silicon layer

contacting said first buried silicon regions;

depositing a second insulating layer over the first insulating layer, the first

polycrystalline silicon layer and the second buried silicon regions; and

depositing a second polycrystalline silicon layer over said second insulating layer

and said second buried silicon regions of the second conductivity type, said second

buried silicon regions of the second conductivity type, said second buried silicon regions

of the second conductivity type being insulated from said second polycrystalline silicon

layer, as required by claim 1.

The prior art, either singly or in combination fails to anticipate or render obvious, the

limitations of:

... forming buried silicon regions of a second conductivity type within the silicon

substrate of the first conductivity type;

depositing a first polycrystalline silicon layer over the silicon substrate of the first

conductivity type; and

depositing a second polycrystalline silicon layer over the silicon substrate of the first conductivity type,

wherein a first portion of said buried silicon regions of the second conductivity type contacts the first polycrystalline silicon layer and is isolated from the second polycrystalline silicon layer, and a second portion of said buried silicon regions is insulated from the first and the second polycrystalline silicon layer, as required by claim 13.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 10/619,981

Art Unit: 2812

Page 4

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walle Linels M July 6, 2004

> /John F. Niebling Supervisory Patent Examiner Technology Center 2800